DESIGN AND IMPLEMENTATION OF SYSTOLIC ARCHITECTURE FOR ADAPTIVE FIR FILTER

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Abstract:

In most of the real time digital signal processing applications like FFT, digital filters etc, multiplication is one of the important operation, which decides the speed of the algorithm. In order to perform matrix multiplication at a greater speed, conventional multipliers are not suitable to achieve the required task. In order to address the above problem and in order to boost up the speed of matrix multiplication, systolic architecture is proposed. The DLMS adaptive algorithm minimizes approximately the mean square error by recursively altering the weight vector at each sampling instance. Here systolic architecture is used to obtain minimum mean square error and updated value of weight vector. Systolic architecture is an arrangement of processor where data flows synchronously across array element.

This project demonstrates an effective design for adaptive FIR filter driven by DLMS algorithm using Systolic architecture, synthesized and simulated on Quartus-II tool in very high speed integrated circuit hardware description language (VHDL) and Field Programmable Gate Arrays (FPGAs). Here, by combining the concept of parallel processing and pipelining into systolic architecture, increases the speed of computation.

Keywords: *Systolic Architecture, DLMS algorithm, LMS Algorithm, VHDL, FPGA, Modelsim,quartus.*

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[I] INTRODUCTION

Adaptive digital filters are mostly used in various signal-processing applications such as channel equalization, echo cancellation, noise cancellation and system identification etc. Many of these applications are based on real-time adaptive filtering to implement the necessary functionalities with desired quality. For such applications the dedicated VLSI systems are used for realization of adaptive digital filters. Amongst the existing Adaptive digital filters, least mean square (LMS)-based finite impulse response (FIR) adaptive filter is the most popular one due to its inherent simplicity, simple structure and better convergence performance. However, the delay in availability of the feedback error for updating the weights according to the LMS algorithm does not favour its pipeline implementation under high sampling rate condition. A large critical-path delay introduces in implementation of LMS adaptive filter due to the feedback path. Therefore, for adaptive filtering of input signal with high sampling-frequency, it is necessary to reduce the critical-path by pipelined implementation. Due to recursive behavior of the conventional LMS algorithm which does not support pipelined implementation, a modified form of LMS algorithm called delayed LMS algorithm which supports pipelined implementation is used.

1.1 Systolic architecture:

Systolic algorithms are parallel versions of sequential algorithms suitable to run on array of processors. Systolic arrays are massively parallel architectures, organized as networks of identical and relatively simple processing elements that synchronously execute operations. Systolic algorithms address the performance requirements of special purpose systems by achieving significant speedup through parallel processing and the prevention of I/O and memory bandwidth. Systolic arrays are finding their way into many practical applications ranging from radar signal processing to low-level image processing problems. The basic concept of systolic architecture is depicted as shown in fig 1.1.

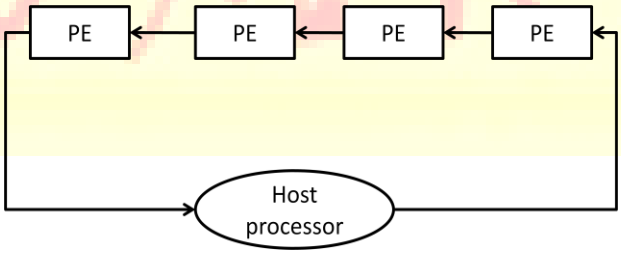

Figure 1.1: Basic Principle of systolic system

1.2 LMS (Least Mean Square) Algorithm

The LMS adaptive algorithm minimizes approximately the mean-square error by recursively altering the weight vector at each sampling instance. Thus an adaptive FIR digital filter driven by the LMS algorithm can be described in vector form as depicted by following equation.

$$y(n)=W^T(n)X(n) \quad \ldots(1.1) \qquad e(n)=d(n)-y(n) \quad \ldots(1.2) \qquad W(n+1)=W(n)+\mu e(n)X(n) \quad \ldots(1.3)$$

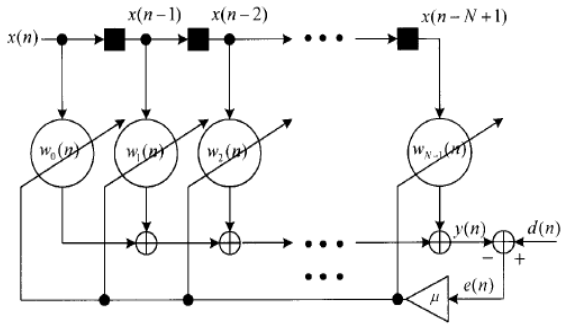

Figure 1.2 : Block diagram of an adaptive FIR digital filter driven by LMS algorithm

Where $d(n)$ and $y(n)$ denote the desired signal and output signal, respectively. The step-size μ is used for adaptation of the weight vector, and e(n) is the feedback error. The tap-weight vector $w(n)$ is define by equation 1.4 and the tap-input vector $x(n)$ is defined by equation 1.5.

$$W(n) = [w_0(n), w1(n), \ldots, wn_{-1}(n)]^T \quad \ldots(1.4)$$

$$X(n) = [x(n), x(n-1), \ldots, x(n-N+1)]^T \quad \ldots(1.5)$$

Where N is the length of an FIR digital filter and $[\bullet]^t$ denotes the transpose operator. The block diagram of the LMS adaptive FIR digital filter is depicted in fig. 1.2 where the symbol ■ denotes the unit delay element. This structure utilizes the algebra for the design of a systolic-array implementation for adaptive filters based on the LMS algorithm. However, since the LMS algorithm contains a feedback loop, the delays created in the decomposition and retiming process prohibit the exact implementation of the algorithm. The design procedure leads to the use of systolic array which implements a special case of the so-called delayed LMS (DLMS) algorithm. The error $e(n)$ used in this algorithm is available only after the processing delay of the systolic array, and thus, the updation of the coefficients is performed with this delay.

1.3 DLMS (Delayed Least Mean Square) Algorithm

LMS algorithm uses the feedback-error corresponding to the n^{th} iteration for updating the filter weights to be used for computing the filter output for the $(n+1)^{th}$ iteration. The DLMS algorithm is similar to the LMS algorithm, except that in case of DLMS algorithm, the weight increment terms to be used in

the current iteration are estimated from the error value and input samples corresponding to a past iteration. The structure of conventional DLMS algorithm is as shown in fig 1.3.The weight update equation algorithm for the DLMS algorithm is given by equation 1.6.

$$W(n+1) = W(n) + \mu e(n-D)X(n-D) \quad \ldots(1.6)$$

here *D* is the number of iterations by which the adaptation is delayed.

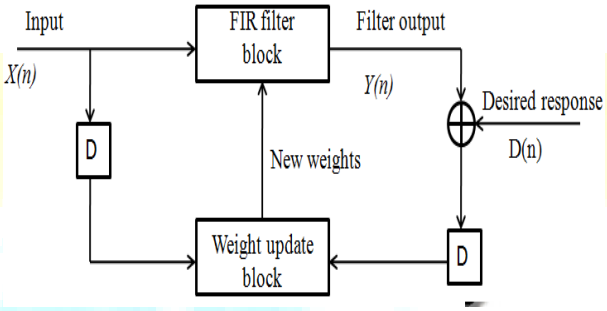

Figure 1.3 : Conventional DLMS algorithm

[II] RELATED WORK

Lots of work is done on systolic architecture and used in different method for design of multiplier, matrix multiplication and for many DSP applications like RLS algorithm, digital FIR filter & adaptive FIR filter using different techniques. one implementation involve systolic array multiplier which was designed for 4 bits using structural and behavioral styles. Thus the design of 4 bit Systolic Array Multiplier in this design was optimized using structural style compared with behavioral style [1]. Another design uses systolic architecture for RLS using FPGA technology with clock getting and used systolic architecture instead of adders, subtracters and multipliers Systolic arrays speed up the processing due to the parallel calculation [2]. Another design uses Systolic Array architecture for Matrix multiplication algorithm .algorithm can be implemented in two methods 1. Conventional method (with-out Pipeline and Parallel Processing) 2. Systolic Architecture (Pipeline and Parallel Processing). In this design the PE was replaced with multiplication and Accumulation (MAC) to enhance the speed and reduce the complexity of Systolic Architecture. The implementation of Matrix Multiplication was done in both methods i.e. Conventional and Systolic Architecture on FPGA. The parallel processing and pipelining was introduced into the proposed systolic architecture to enhance the speed and reduce the complexity of the Matrix Multiplier [3]. This design uses a modified delayed least means square (DLMS) adaptive algorithm to achieve lower adaptation-delay and an efficient pipelined architecture for the implementation of adaptive filter [13]. This design presented a systolic architecture with minimal adaptation delay and input/output latency, thereby improving the convergence behavior to near that of the original LMS algorithm. This design presented a systolic architecture with minimal adaptation delay and input/output latency, thereby

improving the convergence behavior to near that of the original LMS algorithm [16]. This paper presented a design of systolic array architecture for the 1-dimensional Finite Impulse Response adaptive filter. The design was based on the Delayed Least Mean Squares algorithm (DLMS). Performance of the design was analyzed in terms of speed up, adaptation delay and throughput. The different N-tap 1 -D adaptive filters were analyzed and it shows that the proposed scheme was superior in terms of adaptation delay, speed and throughput without the need for additional hardware [14]. In this design realization of adaptive digital FIR filters on a single FPGA chip were presented and the performances of LMS and DLMS algorithms were compared in terms of chip area utilization and filter critical path time [18].

From review of various paper it is observed that most of the researchers have used systolic architecture for the multiplier design, matrix multiplication & many DSP application like RLS algorithm, LMS algorithm and FIR filter. Researchers compared the different architecture of LMS algorithm and obtained improved result in comparison with conventional method.

Therefore in order to perform multiplication more accurately and efficiently use of systolic architecture for design of adaptive FIR (finite impulse response) filter using DLMS algorithm, is a better solution.

[III] PROPOSED WORK

The proposed design uses Systolic Array architecture, which consist of no's of processing element connected to one another. The basic processing element of systolic architecture as shown in fig 3.1.

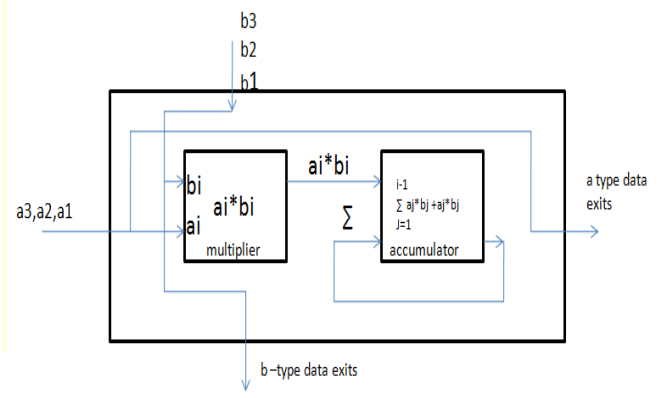

Figure 3.1: PE of systolic Architecture

Where A, B and C are the matrices with order m x k, k x n, and m x n respectively. Each PE of systolic array computes the multiplication of elements and accumulates to the corresponding element and then elements will be passed to neighbor PE in the systolic array. First elements $\alpha_{i,j}$ in row i of matrix A are injected first into PE as pipeline with the sequence $\alpha_{i,k}$ of and the input time to the element of $\alpha_{i+1,j}$ is one time unit later than $\alpha_{i,j}$. Similarly, elements $b_{i,j}$ in column j of matrix B are injected first into PE as

pipeline with the sequence of $b_{k,j}$ and the input time to the element of the sequence of $b_{k,j+1}$is one time unit later than of $b_{k,j}$. The architecture of PE in this approach is shown in fig 3.1 which performs the Multiplication and Accumulation on data.

Fig 3.2 shows the direct forms of DLMS FIR filters, mainly consists adders and multipliers units. The input signals are multiplied by filter coefficients and are gathered together in the adder block. Then it get delayed and obtained the updated value of weight at the same time it get multiplied with input sample and obtain actual output of filter. This actual output is compared with desired output and calculates the error value, the DLMS FIR filter consists of feedback path, this available error through feedback path use for updating of weights of filter. Here multiplication and addition block constitutes a processing element of systolic architecture .

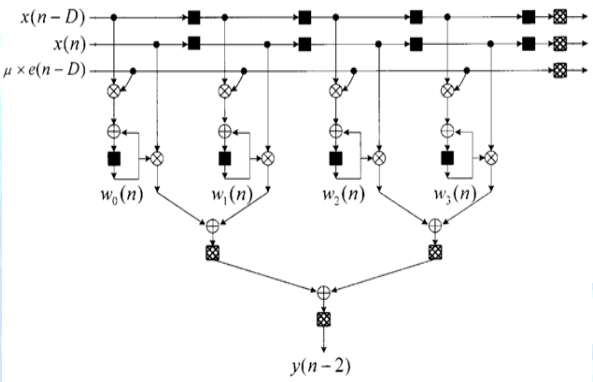

Figure 4.2: systolic architecture for DLMS adaptive FIR filter

Fig 3.3 shows generalized structure of highly realizable systolic architecture for DLMS adaptive digital filter. Where z^{-1} denotes a unit delay, a unit delay is inserted in element in the feedback path for maintaining the lowest critical period. And observe that when *p* is equal to zero this architecture can be reduced to a fully pipelined architecture. On the other hand if *p* is greater than zero this architecture performs better convergence without sacrificing systolic features.

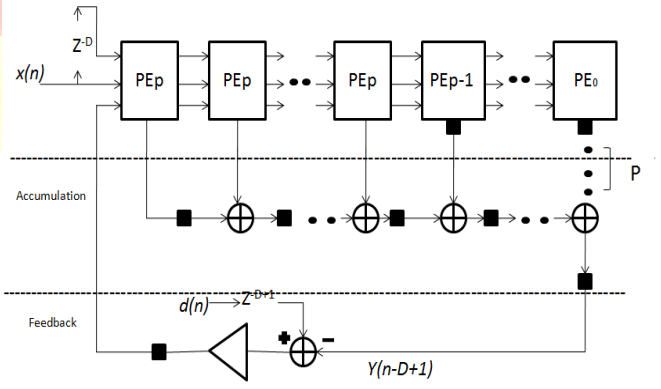

Figure 3.3: Systolic architecture with cascaded systolic-tree PEs

Architecture for realization of Adaptive FIR filter using DLMS algorithm consist of nos. of PE's connected to one another. No of PE's is equal to no's of Taps of an FIR filter, implementation of work involves design for 2-tap, 4-tap, 8-tap, 16-tap, 32-tap FIR filter therefore no's of PE's equal to 2,4,8,16,32 respectively. If taps of filter increase then no's of PE's increase. The architecture is used for obtaining mean square error amd updated value of weight. The MSE obtained is again used for obtaining updated value of weight coefficient, the procedure will continuous until the minimum MSE is achieved. Programming part of the design for systolic Adaptive FIR filter is done using VHDL language and is simulated by using Modelsim software. The design is synthesize by using quartus-II software to obtain the minimum area and lowest critical path for different N-tap FIR filters. Also the comparison of the result in term of speed of convergence by using simple multiplier method and systolic multiplier method is done.

[IV] EXPERIMENTAL RESULTS AND ANALYSIS

First of all the Adaptive filter based on systolic Architecture is desined using very high speed integrated circuit hardware descriptive language (VHDL) and is synthesized and simulated using Quartus-II and Modelsim tool. The code is designed using VHLD language for different N-tap Adaptive FIR filters and is simulated using Modelsim. Simulation result for different N-tap adaptive FIR filter i.e 2-tap, 4-tap, 8-tap, 16-tap, 32-tap respectively are designed and obtain result for input and desired output condition. Initially the filter weights w0, w1, w2, and w3 are assumed to be zero with 8 bit representation to obtain the updated value for reducing the error using the inputs information and error values. The input, desired output is assumed to be 8 bit, again the output from filter and error is assumed to be 16 bit. Weights of filter are changing according to order of filter, if it is 2-tap filter weights are 2, if filter is 4-tap then weights are 4 and so on. In these simulation results the learning factor was assumed to be μ=0.5.

SIMULATION RESULTS

Simulation result for 2-tap, 4-tap, 8-tap, 16-tap and 32-tap adaptive FIR filter is as shown in figures 4.1, 4.2, 4.3, 4.4 and 4.5 respectively.

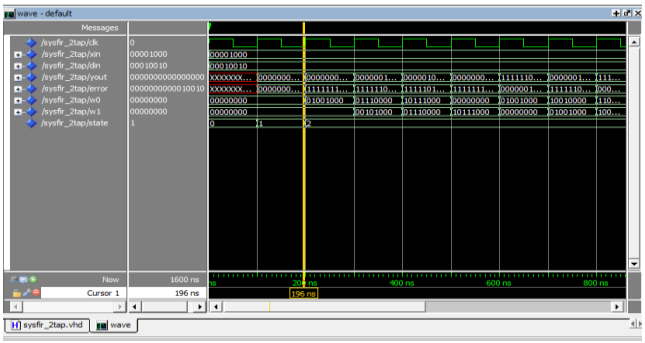

Figure 4.1: Simulation result for 2-tap filter, xin=8 and din=18

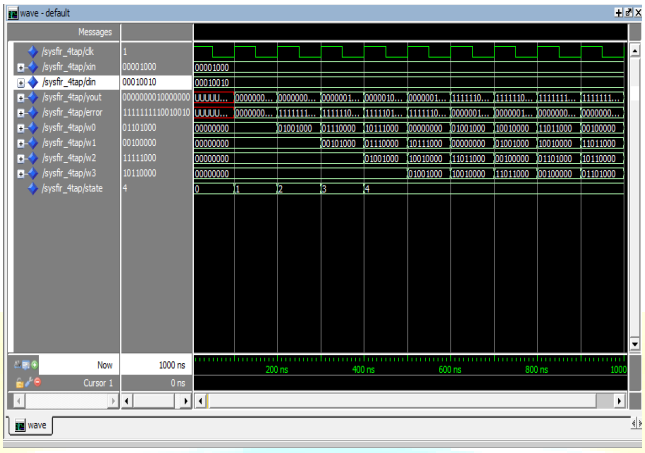

Figure 4.2: Simulation result for 4-tap filter, xin=8 and din=18

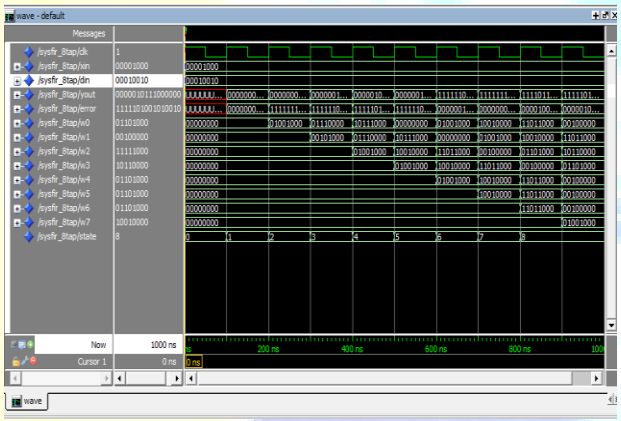

Figure 4.3: Simulation result for 8-tap filter, xin=8 and din=18

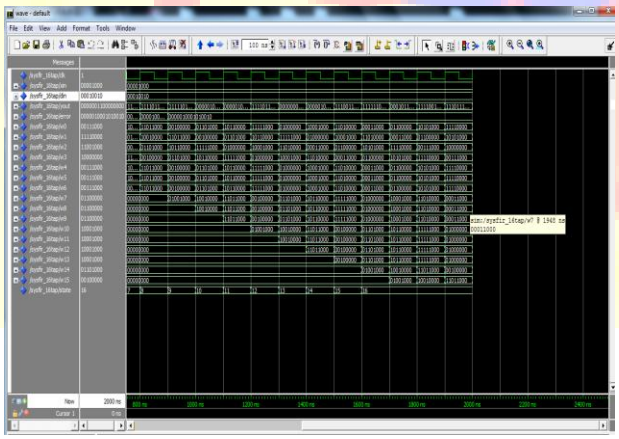

Figure 4.4: Simulation result for 16-tap filter, xin=8 and din=18

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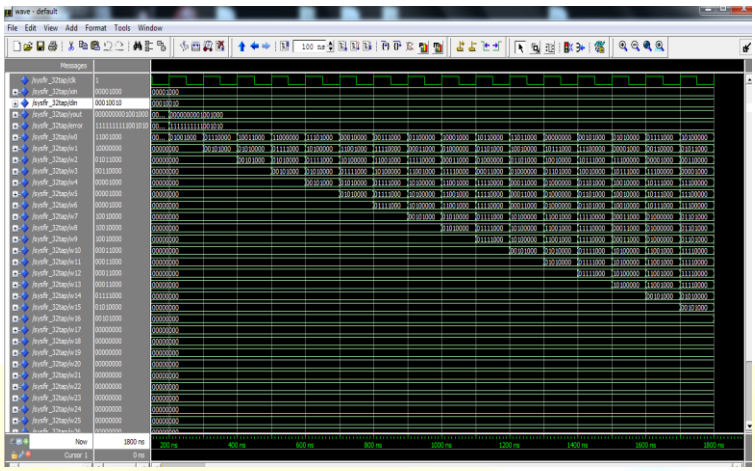

Figure 4.5: Simulation result for 32-tap filter, xin=8 and din=18

SYNTHESIS RESULTS

Synthesis of the design is done using Quartus-II software and obtains the result in term of no's. of ALUTs, total register and critical path for 2-tap, 4-tap, 8-tap, 16-tap, 32-tap DLMS adaptive FIR filter is depicted in table 4.1.

Table 4.1: Synthesis result of N-tap adaptive FIR filter

Nos. of tap's	ALUT'S	Registers	Critical path (ns)
2-Tap	35	25	5.672
4-Tap	90	49	9.221
8-Tap	109	58	9.756
16-Tap	243	131	12.715
32-Tap	353	140	13.426

The graphical representation of the no's of ALUT's in the proposed design and the existing design is as shown in fig. 5.11. It is observed that the number of ALUTs increases by increasing the filter taps. Also the adaptive filter using systolic architecture requires less ALUTs compare to existing design.

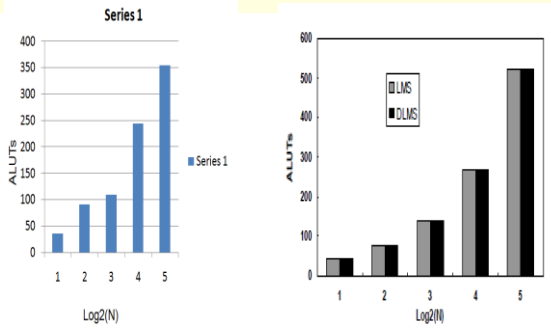

Figure 4.6: comparison of ALUTs of proposed design with existing design

The total number of utilized registers for implementing DLMS adaptive FIR filters with systolic architecture and without systolic architecture is shown in fig.5.12. It is observed that the DLMS adaptive FIR filters without systolic architecture need more registers than DLMS adaptive FIR filters systolic architecture for providing the delay lines.

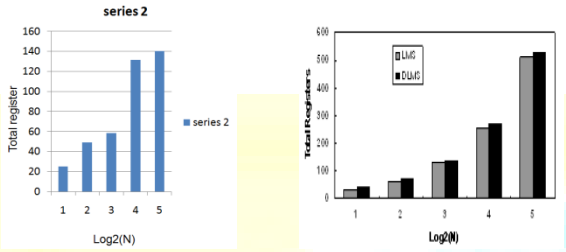

Figure 4.7: comparison of Total registers of proposed design with existing design

Fig 4.8 indicates the comparison of the maximum frequency of DLMS adaptive FIR filters with systolic architecture and without systolic architecture using the critical path time. As shown in fig.5.13 the critical path of DLMS FIR filters without systolic architecture are longer than the DLMS FIR filters with systolic architecture. This means that the DLMS FIR filter with systolic architecture is faster that DLMS FIR filter without systolic architecture designed by using pipeline architecture. Comparison of proposed design (with systolic architecture) is done with existing design (without systolic architecture) and obtains the improved result compared with existing design.

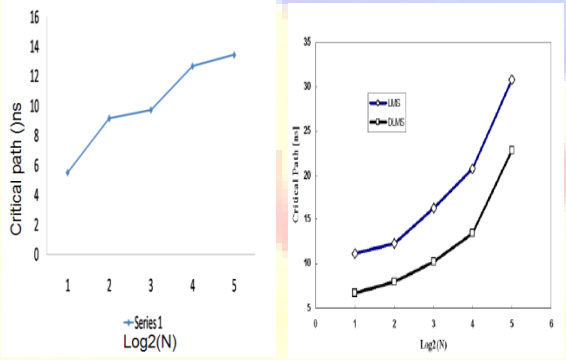

Figure 4.8: comparison of critical path (ns) of proposed design with existing design

[V] CONCLUSION & FUTURE SCOPE

CONCLUSION

Systolic architecture can be used for the design of multiplier, matrix multiplication & many DSP applications like RLS algorithm, LMS algorithm and FIR filter. Low adaptation delay architecture for implementation of DLMS adaptive filter is achieved by using an efficient implementation of systolic architecture. By involving the concept of pipelining and parallel processing into systolic architecture the

adaption delay, chip area and power consumption is reduce by a significant factor. The design is tested and to obtain different parameter like adaption delay chip area and power consumption are estimated for different input and desired output combination. The proposed structure significantly involves less adaption delay chip area and power consumption as compared to the existing structures. Systolic architecture of DLMS algorithm designed using pipeline concept and implemented and achieved the improved result as compared with conventional method.

FUTURE SCOPE

There are many possibilities for further development in this work, this work dealt with adaptive FIR filters using systolic architecture, this is only one of many methods of digital filtering. One can try systolic method for implementation of infinite impulse response (IIR) or lattice filtering which may prove to be more effective in finding minimum mean square error and to reduce noise from input signal. Again this work is done for single input and single output combination, one can try it for multiple input multiple output combination i.e sequence of input.

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