POWER EFFICIENT LOW POWER COLUMN BYPASS MULTIPLIER

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ABSTRACT

Multiplication plays an important role in DSP & communication systems. Nowadays, these two systems are omnipresent in every engineering discipline. Multiplier being a core component of these systems affects their performance i.e. speed, area & power consumption. Hence, there is need of efficient multiplier architecture. The Multiplier is built using adder.

Low power consumption becomes one of the most important criteria for the fabrication of recent DSP and high performance systems. It is known that the multipliers are the main power eating elements of DSP and communication systems. If we can reduce the power consumption of the multiplier block, then we can reduce the power consumption of various digital signal processing chips and communication systems. This type of power efficient multipliers can be developed by reducing switching activities through architecture optimization. Reduction of switching activities through architecture optimization can be done using Column Bypassing Techniques (Turning off some columns in the multiplier array whenever certain multiplicand bits are zero). This paper presents power efficient multiplier structure based on Column Bypassing Techniques. The results shown at the end of this paper shows that there is 20% reduction in power as well as some reduction in memory requirement

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Key words: Switching Activity, Array Multiplier, and Column Bypass Multiplier.

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INTRODUCTION

The computation of a multiplier manipulates two input data to generate many partial products for subsequent addition operations, which in the CMOS circuit design, require many switching activities.[2] Thus, switching activities within the functional units of a multiplier account for the majority of the power dissipation of a multiplier, as given in the following equation : $\mathbf{P_{SWITCHING} = \alpha C V_{dd}^2 f_{clk}}$ ---------- (1)

Where α is the switching activity parameter, C is the loading capacitance, V_{dd} is the operating voltage, and f_{clk} is the operating frequency. αC can also be viewed as the effective switching capacitance of the transistors' nodes on charging and discharging. Therefore, minimizing switching activities can effectively reduce power dissipation without impacting the circuit's operational performance.[3]

This paper presents a low power parallel multiplier, in which switching activities are reduced through architecture optimization, based on **Column Bypassing Technique**. This paper is organized as follows. In the next section we give the information about the basic parallel array multiplier structure. Subsequent sections threw light on Column bypassing technique, and last section gives the comparison of these structures based on power consumption and area overhead.

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BASIC PARALLEL ARRAY MULTIPLIER STRUCTURE

For the multiplication of two unsigned n-bit numbers, the multiplicand $A = a_{n-1}\, a_{n-2} \ldots a_0$ and the multiplier $B = b_{n-1}\, b_{n-2}, \ldots, b_0$, the product $P = P_{2n-1}P_{2n-2}, \ldots, P_0$, can be represented as the following equation:

$$\mathbf{P = P_0\, P_1 \ldots P_{2n-1} = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} (a_i\, b_j)\, 2^{(i+j)}} \quad \text{---------- (2)}$$

To achieve the high-performance demand in DSP applications, the structure of a parallel array multiplier is widely used and a typical array implementation of such a parallel multiplier is the Braun's design as shown in Fig1.

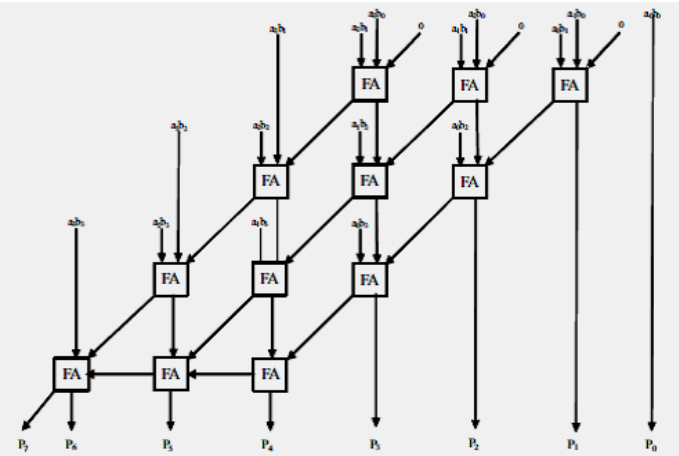


Fig. 1 4x4 Braun multiplier

Drawbacks:

- The number of components required in building the Braun Multiplier increases quadratically with number of bits (a m x n requires mx(n-1) adders & mxn gates). This makes Braun Multiplier **inefficient.**
- The adders of this multiplier performs summation of zero partial products also and, as a result, exhibit **redundant signal switching**. The increased activity in the internal nodes results in **unnecessary power dissipation**.[4]

COLUMN BYPASSING TECHNIQUE

Column Bypassing with reference to multiplier means turning **off** some columns in the multiplier array whenever certain multiplicand bits are zero. In this technique, during working, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0, to save the power. This technique is totally depended on the number of zeroes in the multiplicand bits. The general idea of this technique is depicted in Figure 2.

Consider the multiplication shown in Figure 3, which executes 1010 X 1111. Note that, in the first and third diagonals (enclosed by dashed lines), two out of the three input bits are 0: the "carry" bit from its upper right FA, and the partial product aibj (note that a0 = a2 = 0). As a result, the output carry bit of the FA is 0, and the output sum bit is simply equal to the third bit, which is the "sum" output of its upper FA.

To implement this technique, we have to modify our full adder required in general multiplication. This modified FA for column-bypassing multiplier is shown in Figure 4

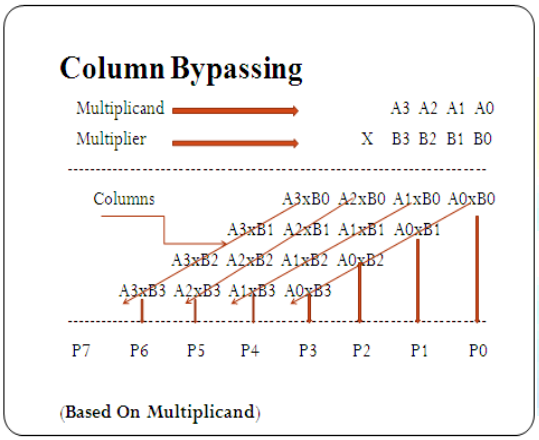


Figure 2:- A Column-Bypassing Technique

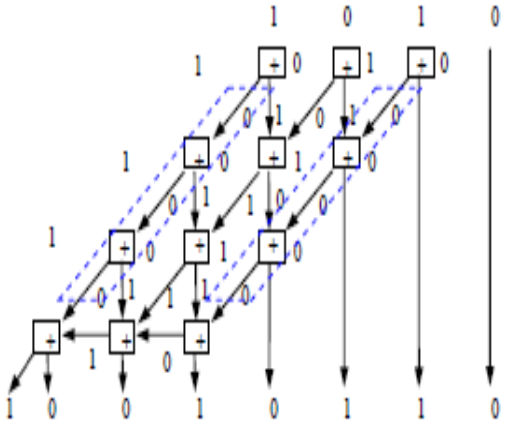


Figure 3:- A Column-Bypassing Example

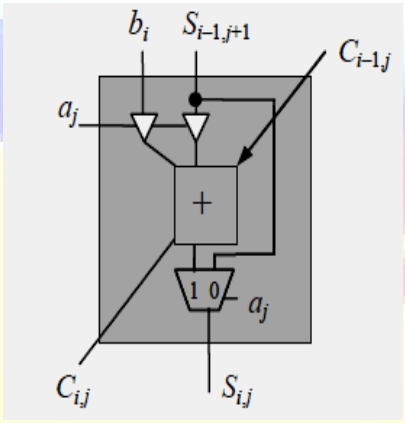


Figure 4: The Modified FA Cell For Column Bypass Multiplier

Based on this, a 4x4 Column Bypass Multiplier structure as shown in Figure 5 is developed. Results for this multiplier structure are given in the subsequent section.

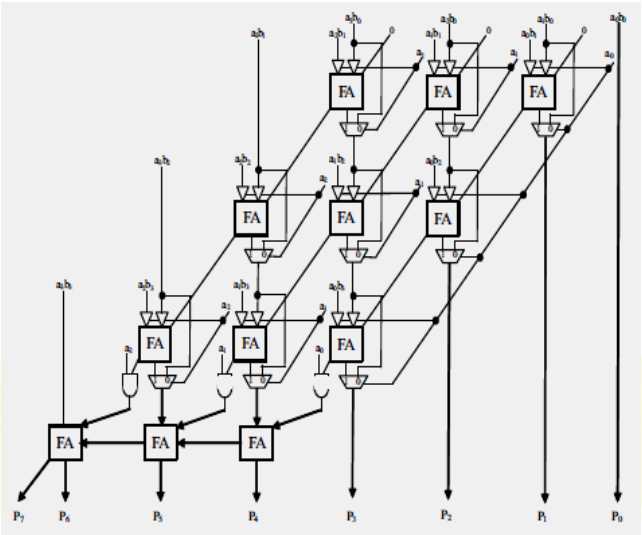
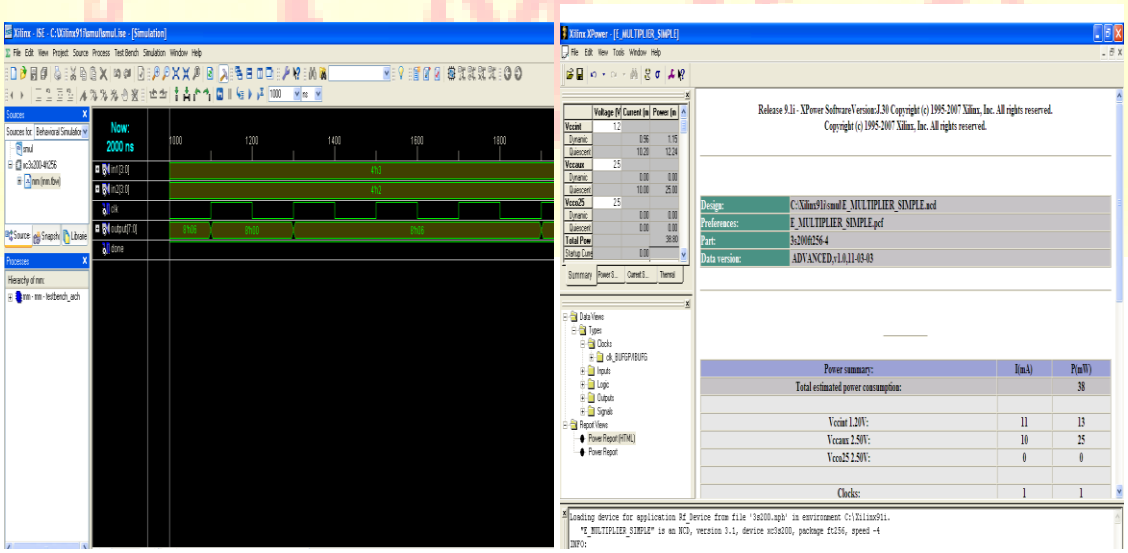


Figure 5: 4x4 Column Bypass Multiplier Structure

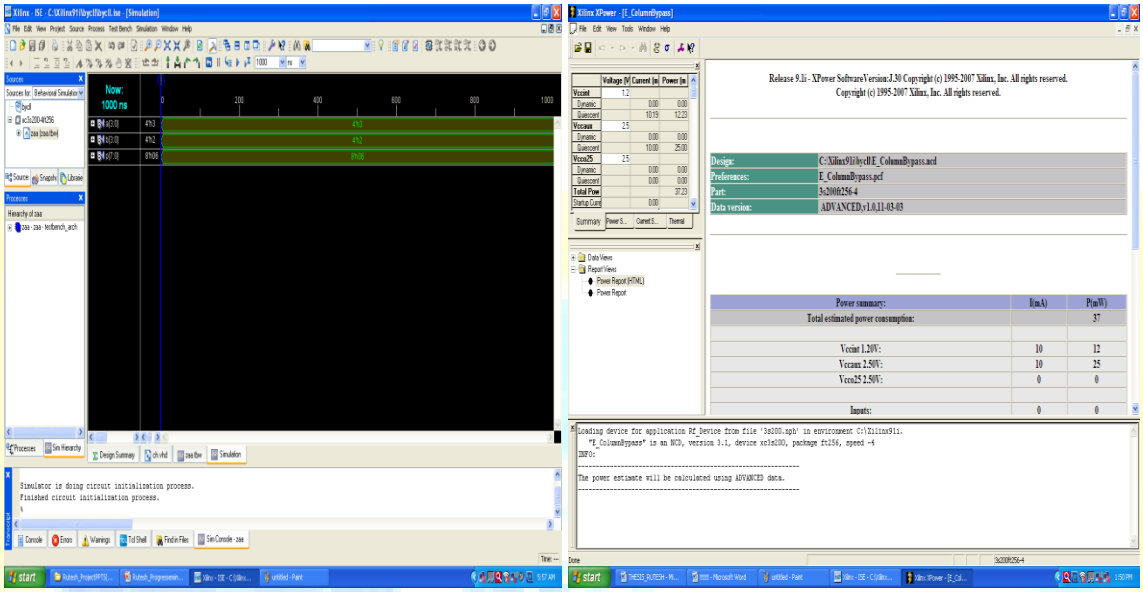
RESULTS

This section shows all results of Simple Array Multiplier (4x4 parallel) shown in fig.1 and 4x4 Column Bypass multiplier for power as shown in fig.5.We have simulated the above designs in Xilinx ISE9.1i and power is calculated using Xpower tool of Xilinx ISE9.1i.We implemented these designs on Spartan 3 FPGA. This section contains Simulation Results, Power Reports, Design Summary, and RTL Schematic for both designs.



(a) (b)

Figure 6: Simulation Result (a) & Power Calculation (b) Of Simple Array Multiplier (4x4) for Multiplication (0011 x 0010)



(a) (b)

Figure 7: Simulation Result (a) & Power Calculation (b) Column Bypass Multiplier (4x4) for Multiplication (0011 x 0010)

SMUL Project Status			
Project File:	smul.ise	Current State:	Placed and Routed
Module Name:	E_MULTIPLIER_SIMPLE	• Errors:	No Errors
Target Device:	xc3s200-4ft256	• Warnings:	38 Warnings
Product Version:	ISE 9.1i	• Updated:	Fri Jul 20 13:37:13 2012

SMUL Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	17	3,840	1%	
Number of 4 input LUTs	40	3,840	1%	
Logic Distribution				
Number of occupied Slices	22	1,920	1%	
Number of Slices containing only related logic	22	22	100%	
Number of Slices containing unrelated logic	0	22	0%	
Total Number of 4 input LUTs	41	3,840	1%	
Number used as logic	40			
Number used as a route-thru	1			
Number of bonded IOBs	18	173	10%	
IOB Flip Flops	8			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	452			
Additional JTAG gate count for IOBs	864			

(a)

BYCLL Project Status			
Project File:	bycl.ise	Current State:	Placed and Routed
Module Name:	E_ColumnBypass	• Errors:	No Errors
Target Device:	xc3s200-4ft256	• Warnings:	2 Warnings
Product Version:	ISE 9.1i	• Updated:	Fri Jul 20 13:42:56 2012

BYCLL Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	33	3,840	1%	
Logic Distribution				
Number of occupied Slices	17	1,920	1%	
Number of Slices containing only related logic	17	17	100%	
Number of Slices containing unrelated logic	0	17	0%	
Total Number of 4 input LUTs	33	3,840	1%	
Number of bonded IOBs	16	173	9%	
Total equivalent gate count for design	198			
Additional JTAG gate count for IOBs	768			

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints		

(b)

Figure 8: Deign Summary of Simple Array Multiplier(4x4)(a) & Column Bypass Multiplier (4x4)(b)

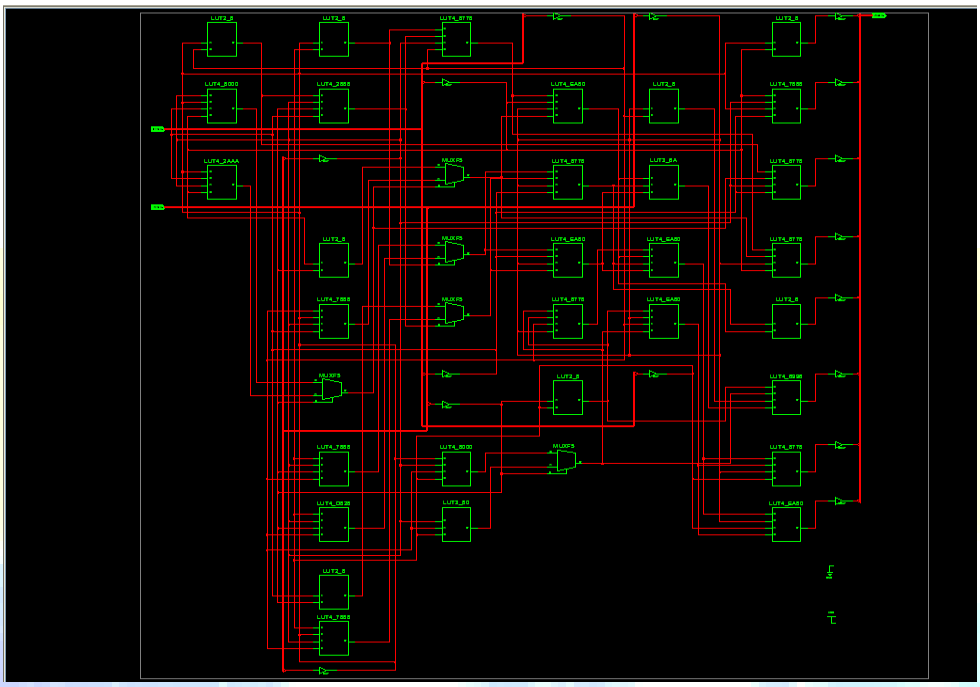


Figure 9: RTL Schematic of Column Bypass Multiplier (4x4)

CONCLUSION

It is found that, for all input combinations, the Simple Array Multiplier requires the same amount of power i.e. 38.77 Mw. It is found that the power consumption of Column Bypass multiplier (for 0011 x 0010) is 37mW which is approximately 2mW less than the Simple Array Multiplier for same input combination. It is also observed that the power consumption of Column Bypass multiplier depends on number of zeros in the input multiplicand as well as position of zero in the multiplicand. It is also found that the power consumption of Column Bypass multiplier [for (A=0000) x B)] is much less than Simple Array Multiplier i.e. 16mW , but not equal to zero. Total memory usage of Simple Array Multiplier is 139580 kilobytes, whereas total memory usage of Column Bypass multiplier is 138440 kilobytes

FUTURE SCOPE

As an attempt to develop arithmetic algorithm and architecture level optimization techniques for low-power multiplier design, the research presented in this dissertation has achieved good results and demonstrated the efficiency of high level optimization techniques.

However, there are limitations in our work and several future research directions are possible. Design can be modified for 8-bit or n- bit operation depending on the requirements. Proposed design is for unsigned multiplication. It can be enhanced for signed operation also. Designed multiplier is for fixed point binary number. It can be modified for floating point binary multiplications

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