COMPARATIVE ANALYSIS OF ULTRA MOSFET WITH CONVENTIONAL MOSFET

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Abstract:

UMOSFET is a power MOSFET. It is called UMOS because its gate region is in U shape, the specific on resistance of the UMOS is significantly smaller than its predecessor DMOSFET as the channel density can be increased can be made larger by using a smaller cell pitch. Unlike DMOSFET it does not have a JEFT region which further reduces the on resistance. A high voltage can be supported by the UMOS structure. The breakdown voltage of the UMOS is significantly larger than ordinary MOSFET. Larger N-drift region allows large amount of currents and also reduces the resistance as the area is increased significantly. The bulk which was a sizable portion of n-channel and p-channel MOSFET is quit thin is UMOS, whereas the drain which makes a small portion in MOSFET occupies a significantly large area and play a major role in the reduction of on resistance and withstanding the high value of voltages.

Using UMOS is saving 40% free space than using NMOS technology. The electric field in the gate oxide is relatively large in the U-MOSFET structure. In addition, the reverse transfer capacitance for the power U-MOSFET structure is much greater than the NMOS.

We are aiming to model a UMOS structure using silvaco and compare its characteristics with an NMOS modeled in silvaco.

Keywords:-MOSFET, VMOSFET, Trench, Silvaco, DMOSFET

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Introduction

The UMOS field effect transistor or UMOSFET is a form of vertical or "trench" style structure used for MOS transistors. This form of semiconductor "trench" or vertical semiconductor technology offers significant advantages in terms of speed and lowering the ON resistance. As a result many manufacturers of semiconductor electronics components offer vertical forms of structure for their MOS transistors.

The UMOS transistor is very similar to the VMOS FET. It is a slightly later development of the same basic principle. UMOSFETs are able to provide a useful function in many relatively high power applications, both in power supplies and as RF power transistors. It can be seen from the diagram of the structure of the UMOS FET, that it is very similar to that of the VMOS FET. The main difference is that the bottom of the V is flattened out to give it a U shape - hence the name UMOS.As with the VMOS FET, where the structure is very similar, the most striking point about the new device is the "U" groove in the structure which is the key to the operation of the device. The "U" groove performs the same function as the "V" groove found in VMOS FETs.

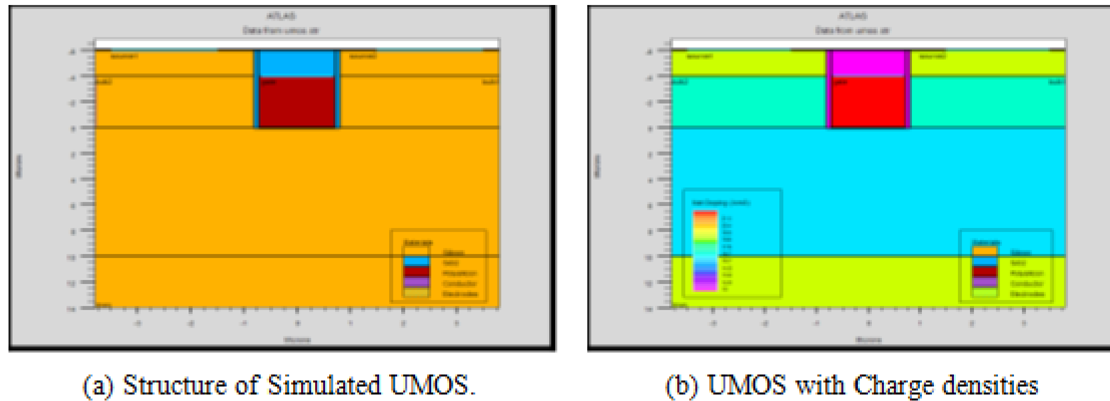
It can be seen that the source is at the top of the device, and the drain is at the bottom. Instead of flowing horizontally as in the standard FET, current in this device flows vertically[1-3].

UMOS Structure

UMOS have the gate trenched into the silicon in U shape as we can see from the Fig 1(a). UMOS is divided into four parts apart source, bulk or substrate, drain which is composed of two regions N- drift and N+ region. The source is a highly doped N+ region. Substrate is a p-type lightly doped region. The major part portion of drain that is N-drift region is a lightly doped region. The bottom most part is a highly doped N+ region. The doping can be done using ion implantation after which a U shaped trench is made into the semiconductor. After the trench is made oxide layer is grown and a gate is deposited in it, since the shape of the gate region is in U it is named as UMOS[6-8].

Figure 1(a) shows the basic structure of a UMOS when it is sliced vertically, it should be noted that the source1 and source2 are connected to each other when we look in a three dimensional

structure however the simulation is done in 2D we will consider them to be separate for the sake of simulation and we will apply same voltage to both source1 and source2 so that they can act as a single entity, similarly the bulk is considered separated into two parts bulk1 and bulk2 for the sake of simulation, however same voltage will be applied so that the effect remains same.



(a) Structure of Simulated UMOS. (b) UMOS with Charge densities

Figure 1: Structure of Simulated UMOS & Charge densities using Silvaco

Figure 1(b) shows the doping concentration and the dimensions of the UMOS. The oxide thickness is taken to be 0.1µm. Source is 2µm thick and the substrate is 4µm. The drift region thickness is 14µm of which 10µm is the N-drift region and the remaining is the N+ region.

The doping profile of the simulated UMOS is as follow. Source is an n-type highly doped region, doping concentration is 10^{-19} cm^{-3}. Substrate is a lightly doped p-type region, doping concentration is 10^{-17} cm^{-3}. N-drift region is a lightly doped n-type region, doping concentration is 10^{-16} cm^{-3}.Then N+ region is a highly doped n-type region, its concentration is 10^{-19} cm^{-3}.

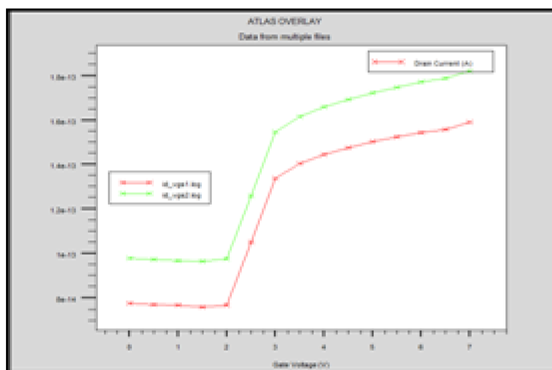
Working of UMOS

When a positive bias is applied to UMOS drain without the application of a gate bias. Junction is formed between the lightly doped p substrate region and the N-drift region, the junction formed is due to the reverse biased as the substrate is connected to ground and a voltage is applied to the drain. N-drift region supports the voltage applied across it. When a positive bias is applied to the gate of UMOS it results in the flow of the drain current, as the application of positive bias on gate produces an inversion layer at the surface of the P substrate along the sidewalls of the gate trench. The inversion layer formed acts as a conductive layer for the movement of electrons from the source terminal to the drain terminal. After moving from the source through the inversion

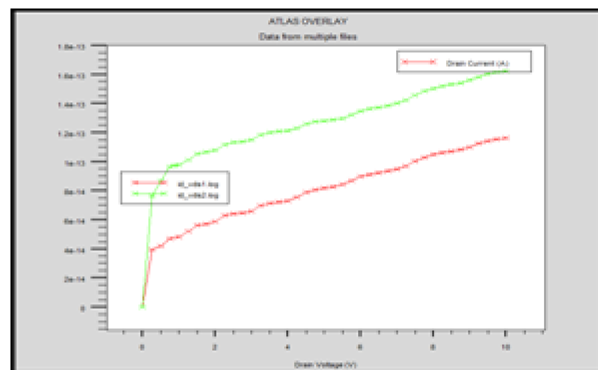
layer, the electrons enter the N-drift region. As the applied bias is positive there will be an accumulation of charges, this accumulation layer at the bottom of the gate surface helps in the distribution of the electrons in the N-drift region. The current spreads from the bottom of the gate to the entire cross section of the N-drift region. However the non-uniform distribution of current will increase the specific on resistance of the UMOS as compared to the N-drift region.

UMOS operates in a blocking mode when the gate is shorted with the substrate, there is a junction formed between the substrate and the drain region, the thickness of the N-drift region determines the level of voltage the UMOS can support as most of the applied voltage is supported by the lightly doped N-drift region. The thickness and the doping concentration of the N drift region allows the user to fabricate device with required breakdown voltage, still a fraction of voltage is supported by the p-substrate. It should be kept in view that p substrate concentration determines the threshold voltage of the UMOS so it cannot be varied to get the desired breakdown voltage, since high threshold voltage will mean high resistance, in order to achieve low resistance the maximum doping concentartion of the substrate has to be limited.

The channel length can be reduced to an optimum value but beyond that optimum value if the thickness is reduced the depletion region will increase and will reach the source, which will result in decrement of the breakdown voltage[4-5].



(a) Input Characteristics of UMOS with Vds as 9V and 12V.



(b) Output characteristics of UMOS with Vgs as 3V and 5V

Figure 2: Input & Output Characteristics of UMOS

Conclusion

UMOS designed and output characteristics simulated are as expected. The device has higher break down voltage. The ON resistance is less than that of DMOS. UMOS can be used as a typical power MOSFET.

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