DESIGNING OF A HALF ADDER USING GRAPHENE P-N JUNCTIONS

P. Teena Kumari*

F. Rajeena*

Ajin.A.S**

Abstract

In this paper, we introduce a Half Adder based on reconfigurable graphene p-n junctions. In this logic device, switching is accomplished by using co-planar split gates that modulate the properties that are unique to graphene, including ambipolar conduction, electrostatic doping, and angular dependent carrier reflection. In addition, the use of these control gates can dynamically change the operation of the device, leading to reconfigurable multi-functional logic.

* Student, Department of Electronics & Communication, Asan Memorial College of Engineering & Technology

** Assistant Professor, Department of Physics, Asan Memorial College of Engineering & Technology

INTRODUCTION

Graphene is a mono-layer of carbon atoms. It shows many remarkable electronic properties such as long electron mean free path, ballistic transport, and high current density. Its Fermi level can be tuned with a gate electrode. These features of graphene offer new opportunities for establishing novel carbon-based nanoelectronic systems that are functionally different from conventional CMOS devices. However, one major challenge of using graphene ribbon is the edge scattering, leading to relatively low mobility [1,2,3].

This paper is organized as follows; In first chapter Graphene p-n junction is described. The second chapter is dealing about reconfigurable graphene logic device and in the third chapter a Half adder is designed using graphene logic device.

GRAPHENE P-N JUNCTIONS

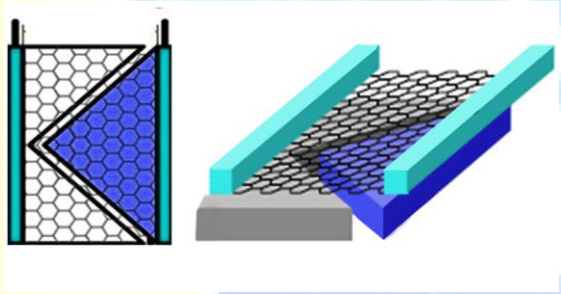

FIGURE 1. Graphene p-n junction

This device is based on electrostatic doping to form graded p-n junctions. The p-n junction is formed using co-planar split gates beneath a graphene sheet. The graphene sheet is laid on a very smooth surface to reduce electron scattering.

By applying opposite biases (negative and positive bias voltages) to the split gates, the Fermi level of the two regions of the graphene sheet will be lowered and raised above the Dirac point, leading to p-type and n-type doping, respectively [5,6].

Electron Transmission Probability

Electrons can exhibit an optics-like behavior on a graphene sheet. The electron transmission probability across the interface is strongly angle-dependent due to wavefunction mismatch and inter-band tunneling. This is given by the equation,

$$T(\theta) = COS^2(\theta).e^{-\pi K_F d \sin^2(\theta)} \qquad (1)$$

Where k_F is the Fermi wave vector, θ is the incident angle between the electron's wave-vector and interface, and d is the gap of the p-n interface. Depending on θ and d, a fraction of electrons will be transmitted through the interface and the rest will be reflected. Therefore, the device can be tuned from the ON state to the OFF state by switching the n-n interface to the angle-dependant p-n interface.

The angle dependent transmission is used to construct multi-functional graphene device. For a large incident angle, the transport through a p-n junction can be highly resistive as most of the carriers will be reflected from the junction. The same junction, however, when doped as either an n-n or p-p interfaces will exhibit a low resistive state as carriers will be transported at the high Fermi velocity. This property will enable us to develop graphene based p-n junctions [5].

RECONFIGURABLE GRAPHENE LOGIC DEVICE

Here the reconfigurable graphene logic circuit consists of a back-to-back p-i-n junctions formed from three split gates with three top contacts made to a single sheet of graphene. Shown in Figure 2.

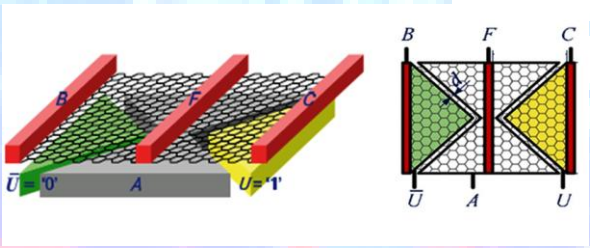

FIGURE 2. Graphene logic circuit

By modifying the voltages on the split gates, the ON/OFF state of the two junctions are switched, establishing different logic functions. Therefore, the proposed graphene logic provides multifunction gates that can be dynamically reconfigured, leading to innovative graphene circuit implementations [6].

Reconfigurable Basic Logic Gates

Here we are constructing a reconfigurable AND, OR & NOT gate using single back-to-back graphene p-i-n junctions. The middle back gate is defined as input A. The left triangular gate is U^I (low voltage) and the right triangular gate is U (high voltage). Middle electrode is the output terminal F while the left electrode is B and the right electrode is C. The structure is shown in Figure 3.

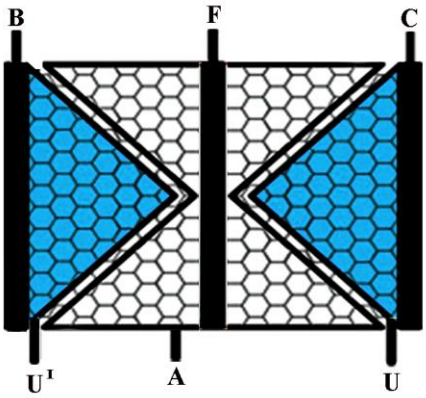

FIGURE 3. Reconfigurable Logic Gates

For a NOT gate A is the input and F is the output terminal. Fix the terminals U=1(U makes the right triangular gate n-type & U^I makes the left triangular gate p-type), B=1 and C=0. When the input A is 1, the middle graphene region becomes n-type. Then the right terminal (C) voltage will come across the output terminal (F), i.e. F=0. But the left p-n junction creates a high resistive state so that the current flow between B & F electrodes is turned off. Alternatively when input A is 0, the middle graphene region becomes p-type and the left terminal (B) voltage will come across the output, i.e. F=1. Therefore it verifies NOT operation.

$$F = \overline{A} \qquad (2)$$

For an AND gate A & C are the inputs and F is the output terminal. Fix the terminals U=1(U makes the right triangular gate n-type & U^I makes the left triangular gate p-type) & B=0. When the inputs A & C are 0, output electrode F connects to the left terminal B, i.e. F=0. But the right side p-n junctions between the electrodes C and F creates a high resistive state so that the current flow between these electrodes is turned off. Similarly when the inputs A=0 & C=1, the output electrode F connects to the left terminal B, i.e. F=0. When the inputs A=1 & C=0, the output electrode F connects to the right terminal C, i.e. F=0. When both the inputs are 1, output electrode F is connects to the right terminal C, i.e. F=1. Therefore it verifies AND operation.

$$F = A \bullet C \qquad (3)$$

For OR gate A & B are the inputs and F is the output terminal. Fix the terminals U=1(left triangular gate is n-type) & C=1. When the inputs A & B are 0, output electrode F connects to

the left terminal B, i.e. F=0. But the right side p-n junctions between the electrodes C and F creates a high resistive state so that the current flow between these electrodes is turned off. Similarly when the inputs A=0 & B=1, the output electrode F connects to the left terminal B, i.e. F=1. When the inputs A=1 & B=0, the output electrode F connects to the right terminal C, i.e. F=1. When both the inputs are 1, output electrode F is connects to the right terminal C, i.e. F=1. Therefore it verifies OR operation.

$$F = A + B \qquad (4)$$

HALF ADDER USING GRAPHENE LOGIC GATES

For this Half adder, we required two back-to-back graphene junctions. Each module consists of three split gates, three electrodes and a single monolayer graphene sheet. To make the p-n junctions, bipolar voltages are required i,e for logic '0' negative voltages are required and for logic '1' positive voltages are required. The half adder operation needs two binary inputs: A and B and two binary outputs: SUM and CARRY.

Module-I gives the output SUM for the Half adder. For module-I, let us assume A and B are the inputs. The middle back gate is defined as input A, the right triangular gate is defined as input B and the left triangular gate is defined as inverted B (B^I). Three electrodes are used in this device, the middle electrode is SUM, it is the output terminal while the left electrode is U (assume U=1) and the right electrode is C (assume C=0). Module I is shown in Figure.4.

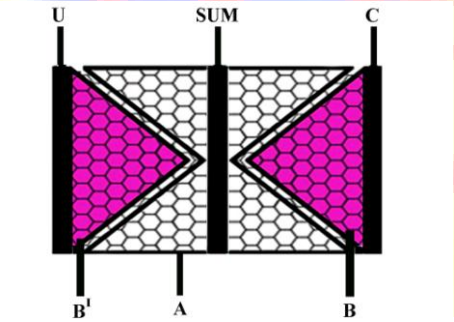

FIGURE 4. Half Adder SUM

Its operation is as follows. Apply the inputs A=0 and B=0 then A and B will become p type. Then the the right terminal (C) voltage will come across the output terminal (SUM). Therefore the output will become low (SUM=0). The p-n junctions between the electrodes U and SUM creates a high resistive state so that the current flow between these electrodes is turned off.

Similarly when the inputs A=0 & B=1, the output will become high (SUM=1), again when the inputs A=1 & B=0, the output will become high (SUM=1), then for the inputs A & B =1, the output will become low (SUM=0).

For module-II gives the output CARRY, let us assume A and B are the inputs. The middle back gate is defined as input B. The right triangular gate is defined as U (assume U=1)and the left triangular gate is defined as inverted U (U^I=0). Then three electrodes are connected to the device, the middle electrode is the output terminal CARRY while the left electrode is C (assume C=0) and the right electrode is A (input).

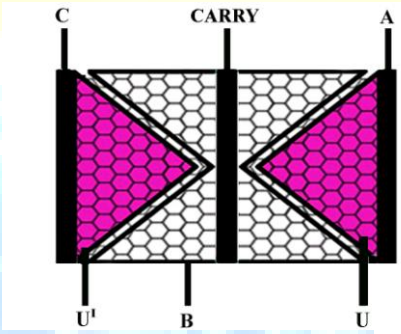

FIGURE 5. Half Adder CARRY

Its operation is as follows. Apply the inputs A=0 and B=0 then A and B will become p-type. Then the left terminal (C) voltage will come across the output terminal (CARRY) therefore the output is low. Similarly when the inputs A=0 & B=1, the output will be low (CARRY=0), again when the inputs A=1 & B=0 and the output will be low (CARRY=0). When the inputs A & B=1 and the output will be high (CARRY=1). Therefore it verifies Half adder operation.

TABLE 1. Half Adder Truth Table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

CONCLUSION

In this paper, we designed a Half adder using graphene reconfigurable logic device based on the control of p-n doping configurations using split gates. By using split gates to change the graphene properties, multi-function logic gate can be obtained and can be dynamically reconfigured.

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