AN EFFICIENT CSLA ARCHITECTURE FOR VLSI HARDWARE IMPLEMENTATION

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Abstract:

Carry select adder (CSLA) is known to be the fastest adder among the conventional adder structures. Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using D latch. Experimental results are compared and the result analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

Keywords- *area efficient, CSLA, low power and BEC*

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I INTRODUCTION:

Area and power have major role in the designing of integrated circuit because of the increase in popularity of portable systems as well as the rapid growth of power density in VLSI circuits. Addition usually influences strongly on the overall performance of digital systems and a crucial arithmetic function. Adders are most widely used in electronic applications. For example, in microprocessors, millions of instructions per second are performed. Due to the increase in the portability of the devices like mobile, laptop etc. require more battery backup. Low power and area efficient addition and multiplication have always been a fundamental requirement of high performance processors and systems. Designing efficient adder is the most difficult problem for researchers in VLSI design.

The carry-select adder (CSLA) provides a compromise between small area but longer delay ripple carry adder (RCA) and larger area with shorter delay carry look-ahead adder [6]. CSLA uses multiple pairs of ripple carry adder (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers (mux) [3].

The modified CSLA using BEC [2, 4, 6] has reduced area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by D latch with enable signal. The proposed architecture reduces the area, delay and power.

This paper is organized as follows; section III presents the detailed structure and the function of the binary to excess-1 converter logic. Section IV and section V explains the regular and modified CSLA respectively. Section VI deals with the proposed architecture. Results are analyzed in the section VII. Section VIII concludes.

II. LITERATURE REVIEW:

Bedriji 1962 proposes [3] that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums. Akhilash Tyagi 1993 introduces a scheme to generate carry bits with block carryin 1 from the carries of a block with block carryin 0 [8]. Chang and Hsiao 1998 [4] propose that instead of using dual carry ripple adder a carry select adder scheme using an add

one circuit to replace one carry ripple adder. Youngioon Kim and Lee Sup Kim 2001 [6] introduces a multiplexer based add one circuit is proposed to reduce the area with negligible speed penalty. Yajuan He et al 2005 proposed an area efficient square root carry select adder scheme based on a new first zero detection logic [5]. Ramkumar et al 2010 proposed a BEC method to reduce the maximum delay of carry propagation in final stage of carry save adder [2].

Ramkumar and Harish 2011 propose [11] BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA. Padma Devi et al 2010 proposed [7] modified carry select adder designed in different stages which reduces the area and power consumption.

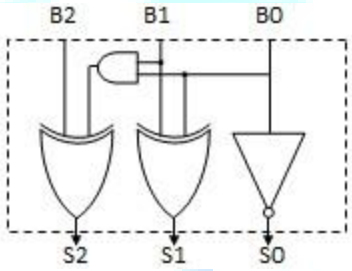

Fig. 1 3-b BEC

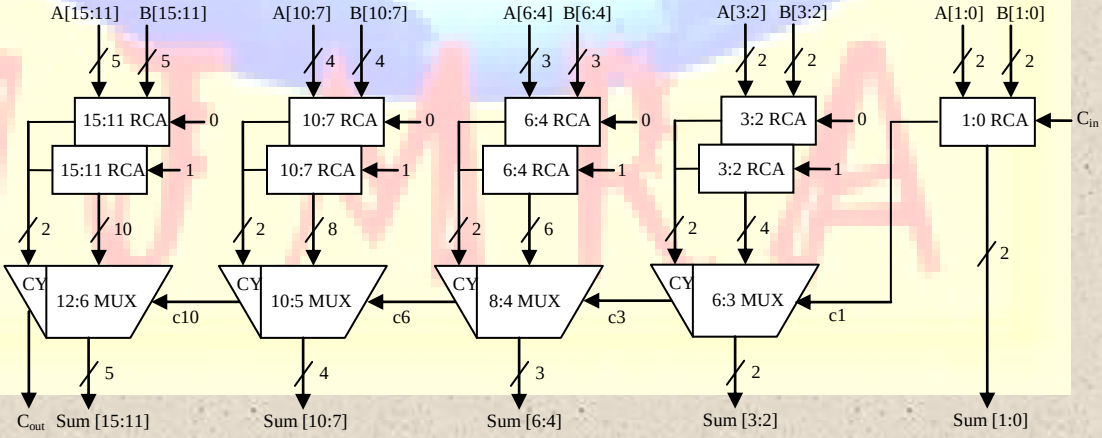

Fig. 2 Regular 16- bit CSLA

Table 1

Function Table of 3-b BEC

B[2:0]	S[2:0]
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

III. Binary to Excess -1 Converter

To reduce the area and power consumption of regular CSLA, RCA with Cin=1 is replaced with BEC [5]. An n+1 bit BEC replaces the n bit RCA. The function table of a 3-b BEC is shown in Fig. 1 and Table 1 respectively [1]. By the use of BEC logic, we can reduce the significant amount of silicon area reduction in the VLSI design. The Boolean expressions of the 3-bit BEC are given below.

S0 = ~ B0

S1 = B0 ^ B1

S2 = B2 ^ (B0 & B1)

IV. REGULAR CSLA ARCHITECTURE:

As said above CSLA compromise between ripple carry adder and carry look ahead adder. The main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The Fig. 2 shows [1] the regular 16-bit carry select adder. It is divided into five groups with different bit size RCA. From the structure of CSLA, it is evident that there is scope for reducing area and power consumption.

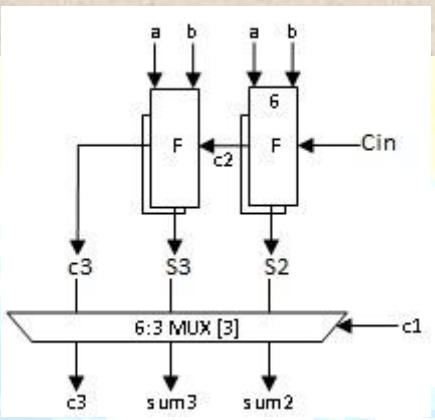

Fig. 3 Group 2

The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer.

Internal structure of the group 2 of regular 16-bit CSLA is shown Fig. 3. By manually counting the number of gates used for group 2 is 57 (full adder, half adder, and multiplexer). One input to the mux goes from the RCA with Cin=0 and other input from the RCA with Cin=1[1].

V. MODIFIED CSLA USING BEC:

The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The modified16-bit CSLA using BEC is shown in Fig. 4 [1]. The structure is again divided into five groups with different

bit size RCA and BEC. The group 2 of the modified 16-bit CSLA is shown Fig. 5. By manually counting the number of gates used for group 2 is 43 (full adder, half adder, multiplexer, BEC).

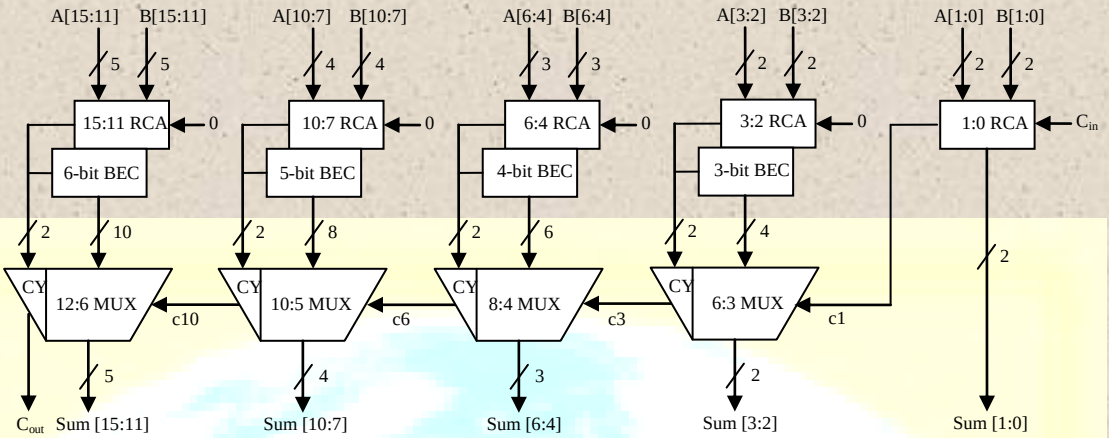

Fig. 4 Modified 16-bit CSLA using BEC

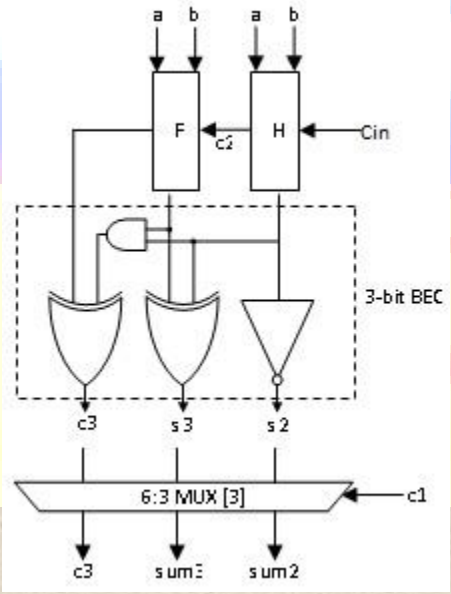

Fig. 5 Group 2

One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 of both regular and modified CSLA, it is clear that BEC structure

reduces the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA [8].

VI. PROPOSED CSLA ARCHITECTURE:

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs. D-latch and it's waveforms are shown in Fig. 6 and Fig. 7 respectively [7].

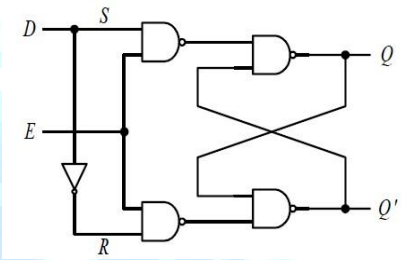

Fig. 6 D-Latch

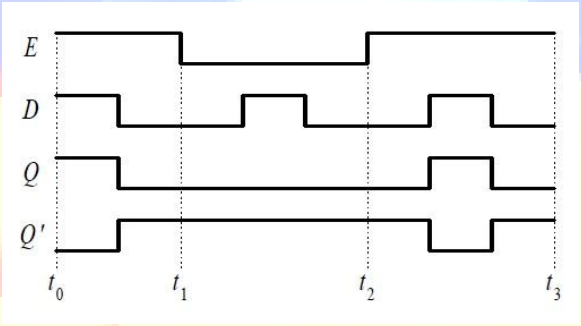

Fig. 7 input and output waveforms

The architecture of proposed 16-b CSLA is shown in Fig. 8. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle.

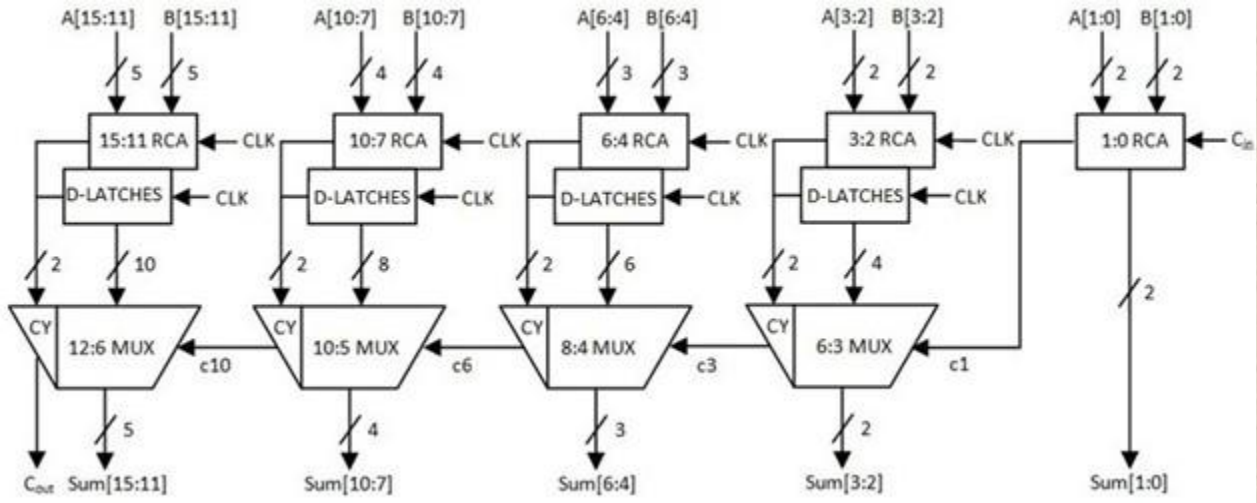

Fig. 8 Proposed 16-bit CSLA

This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, most significant part is 14-bit wide which works according to the clock. Whenver clock goes high addition for carry input one is performed. When clock goes low then carrry input is assumed as zero and sum is stored in adder itself. From the Fig. 9, it can understand that latch is used to store the sum and carry for Cin=1.

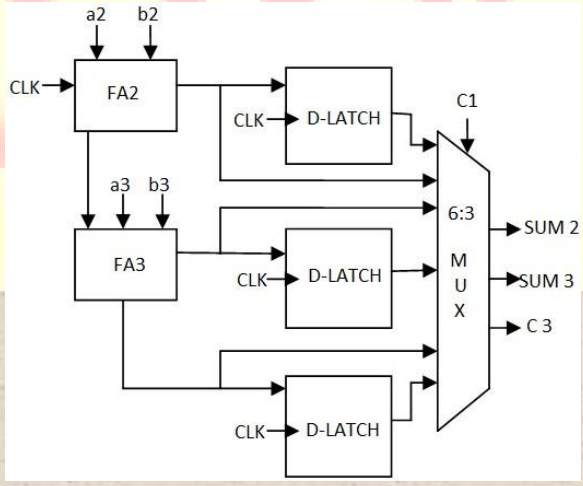

Fig. 9 Group 2

Carry out from the previous stage i.e, least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

The Fig.7 shows the internal structure of group 2 of the proposed 16-bit CSLA. The group 2 performed the two bit addition which are a2 with b2 and a3 with b3. This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2 structure has three D-Latches in which two are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carrry. Multiplexer is used for selecting the actual sum and carry according to the carrry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer.

When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the D-Latch is not enabled. When the clock is high, the addition is performed with carry is equal to one. All the D-Latches are enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

VII. RESULT ANALYSIS:

The 8-bit CSLA is done by the same structure of 16-bit CSLA except group 4 and group 5. The 8^{th} bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit CSLA is done by cascading two 16-bit CSLA and 64-bit CSLA is done by cascading two 32-bit CSLA. Table II exhibits the delay, area and power of regular, modified and proposed CSLA Simulation is carried out using Xilinx simulation tool and Spartan 2E as the target device. The major disadvantage of modified CSLA using BEC is the increasing delay. This disadvantage is overcome in proposed architecture which reduces the delay, area and power than the regular and modified CSLA.

Table II

Comparison of Adders for Delay, Area and Power

Word-Size	Adder	Delay (ns)	Area (no:of gates)	Power (mw)
8-bit CSLA	Regular	14.26	192	196
	Modified	16.06	162	183
	Proposed	12.25	63	99
16-bit CSLA	Regular	17	438	317
	Modified	21.35	384	268
	Proposed	13.50	110	156
32-bit CSLA	Regular	27.97	870	53
	Modified	35.44	762	446
	Proposed	26.66	726	382
64-bit CSLA	Regular	53.82	1698	869
	Modified	63.61	1518	765
	Proposed	47.36	1446	640

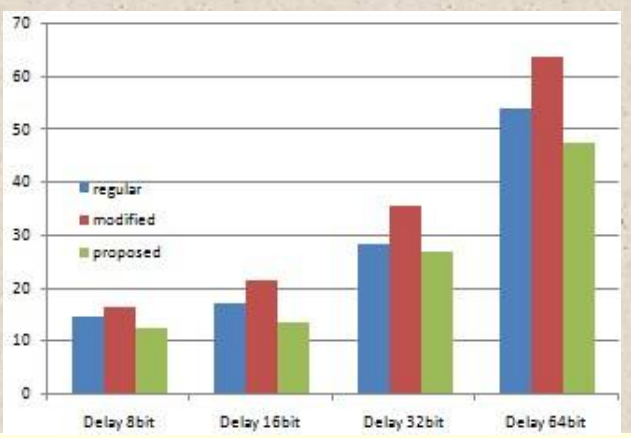

Fig. 10 comparison of adders for delay

The results depicted in Fig. 10 shows that the proposed CSLA has higher speed when compared to regular and modified CSLA.

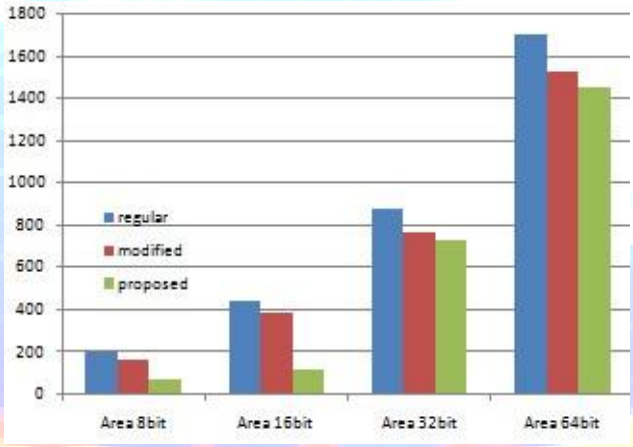

Fig. 11comparison of adders for area

Fig. 12 comparison of adders for power

Figure 11 compares the adder circuit for area comparison. When compared to regular and modified CSLA the proposed circuit occupies less area. In addition to realization of higher speed and lesser area as discussed above, Fig. 12 depicted that the proposed architecture consumes less power when compared to the regular and modified CSLA. The proposed CSLA overweighs both the regular and modified CSLA in terms of area, delay and power.

VIII. CONCLUSION:

A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. Regular CSLA suffers from the disadvantage of occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of D-latches.

ACKNOWLEDGEMENT:

The authors thank the Management and Principal of Sri Ramakrishna Engineering College, Coimbatore for providing excellent computing facility and encouragement for the completion of this work.

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