

REAL TIME IMPLEMENTATION OF IMAGE CRYPTOGRAPHY USING ADVANCED ENCRYPTION STANDARD

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Abstract—

Security in transmission storage of digital images has its importance in today's image communications and confidential video conferencing. Due to the increasing use of images in industrial process, it is essential to protect the confidential image data from unauthorized access. Advanced Encryption Standard (AES) is a well known block cipher that has several advantages in data encryption. However, it is not implemented in real-time applications such as image, video or audio cryptography. In this paper, we present a modification to the Advanced Encryption Standard (MAES) to reflect a high level security and better encryption for image. The modification is done by adjusting the using Block RAM which can be implemented using megawizard function in Quartus IDE. Detailed results in terms of security analysis and implementation are given. Experimental results verify and prove that the proposed modification to image cryptosystem is highly secure from the cryptographic viewpoint.

Keywords – *AES, encryption, decryption, Rijndael, block cipher*

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Introduction

In digital world, encryption is emerging as a disintegrable part of all communication networks and information processing systems, for protecting both stored and in transit data. Encryption is the transformation of plain data (known as plaintext) into unintelligible data (known as ciphertext) through an algorithm referred to as cipher. There are numerous encryption algorithms that are now commonly used in computation, but the U.S. government has adopted the Advanced Encryption Standard (AES) to be used by Federal departments and agencies for protecting sensitive information. The National Institute of Standards and Technology (NIST) has published the specifications of this encryption standard in the Federal Information Processing Standards (FIPS) Publication 197.

The AES is a subset of a much larger encryption algorithm known as *Rijndael*, which was one of many proposals to the NIST competing for becoming a standard encryption algorithm. On October of 2000, the NIST announced the *Rijndael* algorithm as the winner due to the best overall score in security, performance, efficiency, implementation capability and simplicity. The AES algorithm is a *symmetric* cipher. In symmetric ciphers, a single secret key is used for both the encryption and decryption, whereas in asymmetric ciphers, there are two sets of keys known as private and public keys. The plaintext is encrypted using the public key and can only be decrypted using the private key.

In addition, the AES algorithm is a *block* cipher as it operates on fixed-length groups of bits (blocks), whereas in *stream* ciphers, the plaintext bits are encrypted one at a time, and the set of transformations applied to successive bits may vary during the encryption process. The AES algorithm operates on blocks of 128 bits, by using cipher keys with lengths of 128, 192 or 256 bits for the encryption process. Although the original Rijndael encryption algorithm was capable of processing different blocks sizes as well as using several other cipher key lengths, but the NIST did not adopt these additional features in the AES

The AES cipher either operates on individual bytes of the State or an entire row/column. At the start of the cipher, the input is copied into the State as described in Section 2.2. Then, an initial Round Key addition is performed on the State. Round keys are derived from the cipher key using the Key Expansion routine. The key expansion routine generates a series of round keys for each round of transformations that are performed on the State.

The transformations performed on the state are similar among all AES versions but the number of transformation rounds depends on the cipher key length. The final round in all AES versions differs slightly from the first N_r transformation performed on the State. Each round of AES cipher (except the last one) consists of all the following transformation:

- SubBytes()
- ShiftRows()
- MixColumns()
- AddRoundKey ()

The AES cipher is described as a pseudo code in Figure 2. [1] As shown in the pseudo code, all the N_r rounds are identical with the exception of the final round which does not include the MixColumns transformation. The array $w[]$ represents the round keys that are generated by the key expansion routine. In the following sections, individual transformations that are used in each encryption round are described.

Pseudo noise sequences (PN sequences), also referred to as pseudorandom sequences. PN sequence generator block generates a sequence of pseudo random binary numbers using linear feedback shift register (LFSR). Pseudo noise sequence can be used in a scrambler and descrambler. LFSR (linear feedback shift register) is a shift register with a certain number of memory elements. Pseudo noise sequence is a bit stream of '0's and '1's occurring randomly.

Applications of PN sequences include signal synchronization, navigation, radar ranging, random number generation, spread-spectrum communications, multipath resolution, cryptography, and signal identification in multiple-access communication systems. In cryptography, pseudo random noise is a signal which satisfies one or more of the standard tests for statistical randomness

II. DESCRIPTION OF AES ALGORITHM

The AES algorithm is a symmetric block cipher that can encrypt and decrypt information.

Encryption converts data to an unintelligible form called cipher-text. Decryption of the cipher-text converts the data back into its original form, which is called plain-text.

A. AES encryption

The AES algorithm operates on a 128-bit block of data and executed $N_r - 1$ loop times. A loop is called a round and the number of iterations of a loop, N_r , can be 10, 12, or 14 depending on the key length. The key length is 128, 192 or 256 bits in length respectively.

The first and last rounds differ from other rounds in that there is an additional AddRoundKey transformation at the beginning of the first round and no MixColumns transformation is performed in the last round.

In this paper, we use the key length of 128 bits (AES-128) as a model for general

explanation.

BLOCK DIAGRAM:

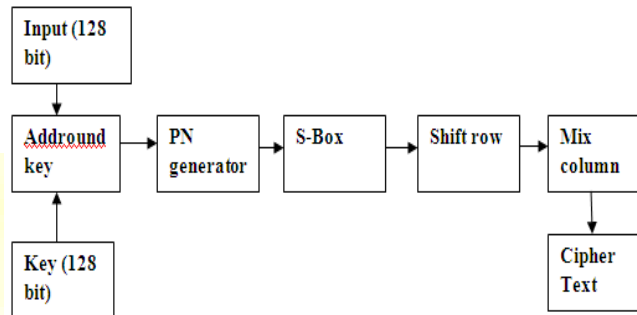


Figure 1 Block diagram for encryption

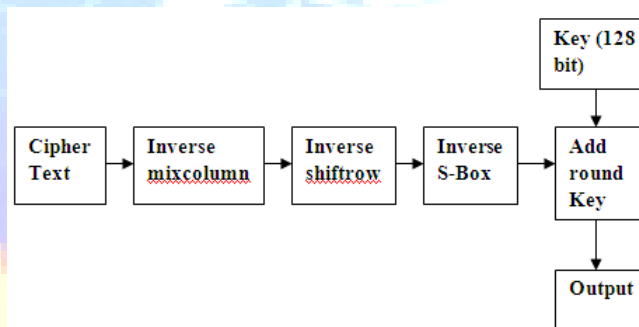


Figure 2 Block diagram for decryption

SubBytes Transformation:

The SubBytes transformation is a non-linear byte substitution, operating on each of the state bytes independently. The SubBytes transformation is done using a once-pre-calculated substitution table called S-box. That S-box table contains 256 numbers (from 0 to 255) and their corresponding resulting values. In this design, we use a look-up table as shown in Table 1. This is a more efficient method than directly implementing the multiplicative inverse operation followed by affine transformation.

Y															
0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f

	0	6	7	7	7	f	6	6	c	3		6	2		d	a	7
	1	c	8	c	7		5	4	f	a	d	a		9	a	7	c
	2	b	f	9	2	3	3	f	c	3	a	e	f	7	d	3	1
	3		c	2	c	1	9		9		1	8	e	e	2	b	7
	4	9	8	2	1	1	6	5	a	5	3	d	b	2	e	2	8
	5	5	d		e	2		b	5	6	c	b	3	4	4	5	
	6	d		a	f	4	4	3	8	4	f		7	5	3	9	a
	7	5	a	4	8	9	9	3	f	b	b	d	2	1		f	d
X	8	c	0	1	e	5	9	4	1	c	a	7	3	6	5	1	7
	9	d	c	3	c	f	7	4	7	4	7	e	d	4	d	9	3
	a	6	8	4	d	2	2	9	8	4	e	b	1	d	5	0	d
	b	e	3	3	0	4		2	5	c	d	a	6	9	9	e	7
	c	0	2	a	a	9	6	4	c	2	3	c	2	1	5	4	9
	d	e	c	3	6	8	d	4	a	6	5	f	e	6	7	a	
	e	7	8	7	d	d	5	e	9	c	6	4	a	5	a	e	8
	f	b	7	2	2	1	a	b	c	e	d	7	1	4	b	8	8
		a	8	5	e	c	6	4	6	8	d	4	f	b	d	b	a
		7	3	b	6	4		f	0	6	3	5	b	8	c	1	9
		0	e	5	6	8	3	6	e	1	5	7	9	6	1	d	e
		e	f	9	1	6	d	8	9	9	1	8	e	c	5	2	d
		1	8	8	1	9	9	e	4	b	e	7	9	e	5	8	f
		8	a	8	0	b	e	4	6	4	9	2	0	b	5	b	1
		f	c	1	9	d	f	6	2	8	1	9	d	f	0	4	6



Table 1 S-Box

ShiftRows Transformation:

In ShiftRows transformation, the rows of the state are cyclically left shifted over different offsets. Row 0 is not shifted; row 1 is shifted one byte to the left; row 2 is shifted two bytes to the left and row 3 is shifted three bytes to the left.

MixColumns Transformation:

In MixColumns transformation, the columns of the state are considered as polynomials over GF (2⁸) and multiplied by modulo x⁴ + 1 with a fixed polynomial c(x), given by: c(x)={03}x³ + {01}x² + {01}x + {02}.

AddRoundKey Transformation:

In the AddRoundKey transformation, a Round Key is added to the State - resulted from the operation of the MixColumns transformation by a simple bitwise XOR operation. The Round Key of each round is derived from the main key using the KeyExpansion algorithm. The encryption/decryption algorithm needs eleven 128-bit RoundKey, which are denoted RoundKey[0] RoundKey[10] (the first RoundKey [0] is the main key).

B. AES decryption

Decryption is a reverse of encryption which inverse round transformations to computes out the original plaintext of an encrypted cipher-text in reverse order. The round transformation of decryption uses the functions AddRoundKey, InvMixColumns, InvShiftRows, and InvSubBytes successively.

AddRoundKey:

AddRoundK
 ey is its own inverse
 functio because function its
 n e theXOR is own

inverse. The round keys have to be selected in reverse order. The description of the other transformations will be given as follows.

InvShiftRows Transformation:

InvShiftRows exactly functions the same as ShiftRows, only in the opposite direction. The first row is not shifted, while the second, third and fourth rows are shifted right by one, two and three bytes respectively.

InvSubBytes transformation:

The InvSubBytes transformation is done using a once-pre-calculated substitution table called InvS-box. That InvS-box table contains 256 numbers (from 0 to 255) and their corresponding values. InvS-box is presented in Table 2.

		Y															
		0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
X	0	5	6	d	3	3	a	3	b	4	a	9	8	f	d		
	2	9	a	5	0	6	5	8	f	0	3	e	1	3	7	fb	
	1	7	e	3	8	9			8	3	8	4	4	c	d	e	c
	c	3	9	2	b	2f	ff	7	4	e	3	4	4	e	9	b	
	2	5	7	9	3	a	c	2	3	e	4	9	0	4		c	4
	4	b	4	2	6	2	3	d	e	c	5	b	2	fa	3	e	
	3		2	a	6	2	d	2	b	7	5	a	4	6	8	d	2
	8	e	1	6	8	9	4	2	6	b	2	9	d	b	1	5	
	4	7	f		6	8	6	9	1	d	a	5	c	5	6	b	9
	2	8	6	4	6	8	8	6	4	4	c	c	d	5	6	2	
5	6	7	4	5		e	b	d	5	1	4	5	a	8	9	8	
c	0	8	0	fd	d	9	a	e	5	6	7	7	d	d	4		
6	9	d	a		8	b	d	0	f	e	5		b	b	4		
0	8	b	0	c	c	3	a	7	4	8	5	8	3	5	6		
7	d	2	1		c		0		c		b			1	8	6	
0	c	e	8f	a	3f	f	2	1	af	d	3	1	3	a	b		
8	3	9	1	4		6	d	e	9	f		c	f	b	e	7	
a	1	1	1	4f	7	c	a	7	2	cf	e	0	4	6	3		
9	9	a	7	2	e	a	3	8	e	f	3	e	1	7		6	
6	c	4	2	7	d	5	5	2	9	7	8	c	5	df	e		
a	4	f	1	7	1	2	c	8	6	b	6	0	a	1	b	1	
7	1	a	1	d	9	5	9	f	7	2	e	a	8	e	a		

b	fc	6	e	b	6	2	9	0	a	b	0	fe	8	d	a	f4
c	1	d	a	3	8		c	3	b	1	1	5	2	8	e	
d	6	5		a	1	b	4	0	2	e	7	9	9	c	9	
e	0	1	7f	9	9	5	a	d	d	5	a	f	3	9	c	ef
f	0	0	b	d	e	a	5	0	8	b	b	c	3	3	9	1
	1	2		7	b	7	d	2	e	6	1	6	5	2	0	7
	7	b	4	e	a	7	6	6	1	9	4	3	5	1	c	d

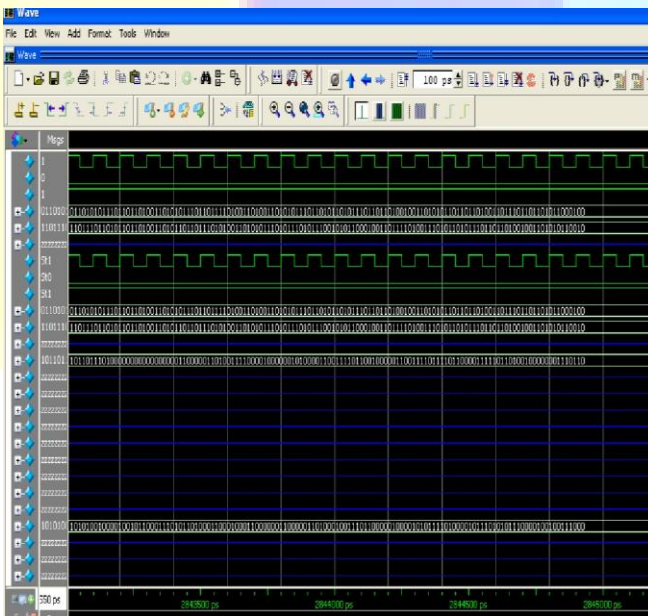
Table 2 Inverse S-Box

InvMixColumns Transformation:

In the InvMixColumns transformation, the polynomials of degree less than 4 over GF(2⁸), which coefficients are the elements in the columns of the state, are multiplied modulo (x⁴+ 1) by a fixed polynomial d(x) = {0B}x³ + {0D}x² + {09}x + {0E}, where {0B}, {0D}; {09}, {0E} denote hexadecimal values.

III Simulation Results

The design has been coded by Verilog HDL. All the results are simulated using on the Quatus II, the Model Sim – 6.6c.



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Figure 3 Output for encryption

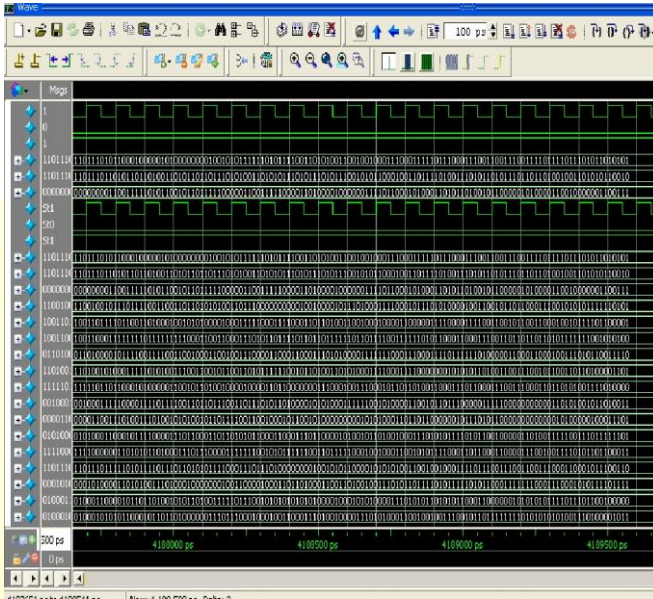


Figure 4 Output for decryption

IV Conclusion

The AES (Advanced Encryption Standard) architecture for the 128 bit data length and 128-bit key length was designed using Verilog and synthesized with RTL Compiler, physically designed with SOC quartus. With the proposed novel architecture, and fully sub-pipelining, prototyped III FPUA's and then ASIC design was throughput has increased to 58.18 Gbps. The design was prototyped in FPGA's and then ASIC design was made for 90nm Technology. This design has a scope of using in portable devices, where bulk transmission of data is required with high security

V Future Work

The implementation of combinational s-box circuit to avoid the LUT(Look up table). It will reduce both Static and dynamic power upto 75% and compare to existing system.

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